LISTING OF CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A process for ~~the firm connection of~~connecting processed semiconductor wafers, wherein~~, in the case of more than~~ at least two wafers~~, the wafers~~ are located in a ~~central area~~mid position of ~~the~~a stack of wafers, and wherein in an operation of a ~~mechanically firm~~mechanical connecting, electrically insulating connections ~~(6, 6a, 6b)~~ and electrically conductive connections ~~(5)~~ are produced between ~~the~~at least two semiconductor wafers, said process comprising ~~at least the following operations~~:

applying structured layers of electrically non-conducting and electrically conducting glass paste on ~~respectively one of the~~ two wafer sides of said two wafers to be connected ~~with each other~~;

conditioning and premelting of the glass pastes;

geometrical alignment of the two wafers to be connected;

joining ~~of~~ the wafers at a processing temperature of the ~~glasses of~~ glass pastes using a mechanical pressure.

2. (Currently Amended) The process according to claim 1, wherein the glass pastes~~, in particular glass solders~~ are applied ~~with~~by a screen printing process.

3. (Currently Amended) The process according to claim 1, wherein that the non-conducting~~, low-melting~~ glass paste and the electrically conducting glass paste have different conditioning and premelting conditions and ~~that, consequently, the~~therefore conditioning and premelting are implemented successively, each in a ~~respectively~~in a separate process.

4. (Currently Amended) The process according to claim 1, ~~wherein~~wherein that the non-conducting~~, low-melting~~ glass paste and the electrically conducting glass paste have substantially the same processing temperature.

5. (Currently Amended) The process according to claim 1, wherein the ~~low-melting~~non-conductive glass paste and the electrically conducting glass paste have different processing temperatures and these are successively passed in a process.

6. (Currently Amended) The process according to claim 1, wherein at least one of the two wafers is electrically connected in an area that is not structured electronically as an area of ~~the~~a starting material of the wafer.

7. (Currently Amended) The process according to claim 1, wherein the wafers are electrically connected at specific ~~switching~~electric circuit points in electronically structured areas.

8. (Currently Amended) The process according to claim 1, wherein ~~the~~a connection formation of the ~~connections of the~~ glass pastes takes place at a temperature in a range of ~~less than~~ 450°C.

9. (Currently Amended) The process according to claim 1 ~~and any of the subsequent claims, characterized in that~~wherein the electric connection of ~~the~~a substrate ~~for~~of an SOI ~~wafers~~wafer is implemented through previously produced openings in a buried oxide layer and in an active silicon layer~~, in particular the wall areas of the opening of the active silicon layer being provided with an insulating layer (7a) prior to the electric connection~~.

10. (Cancelled)

11. (Currently Amended) A process for ~~the firm connection of~~bonding processed semiconductor wafers as system wafer ~~(1)~~ supporting ~~microelectromechanical~~micro-electromechanical or electronic structures with a cover wafer ~~(2)~~ also supporting electronic structures, wherein in an operation of ~~a mechanically firm connecting~~bonding, electrically insulating connections and electrically conductive connections are produced between the semiconductor wafers, said process comprising ~~at least the following steps~~:

applying a first electrically non-conducting, structured layer and a second electrically conducting structured layer ~~of respectively~~, each one with a glass paste ~~(5, 6)~~ on at least one face of the ~~two~~ wafers ~~(1, 2)~~ to be ~~connected with each other~~;bonded together,

conditioning of the glass pastes;

geometrical alignment of the wafers ~~(1, 2)~~ to be ~~connected~~bonded;

joining ~~of~~ the wafers ~~(1, 2)~~together at a processing temperature of the glass pastes using a mechanical pressure.

12. (Currently Amended) The process according to claim 11, wherein the glass pastes ~~(5, 6) are glass solders and~~ are applied with a screen printing process.

13. (Currently Amended) The process according to claim 11, wherein the non-conducting, glass paste is low-melting ~~glass paste (6, 6a)~~ and the electrically conducting glass paste ~~(5) have one of~~has a different ~~conditioning and~~ premelting ~~conditions~~condition and ~~the conditioning or~~ premelting of each of the pastes is implemented successively in a ~~respective~~ separate process.

14. Currently Amended) The process according to claim 11, wherein the non-conducting, glass paste is low-melting ~~glass paste (5)~~ and the electrically conducting glass paste ~~(6) have~~has a substantially ~~the~~ same processing temperature.

15. (Currently Amended) The process according to claim 11, wherein the non-conducting~~,~~ glass paste is low-melting ~~glass paste (5)~~ and the electrically conducting glass paste ~~(6) have~~has a different processing temperatures ~~and these temperatures are successively passed in the process~~.

16. (Currently Amended) The process according to claim 11, wherein at least one of the wafers is electrically connected in ~~an~~a wafer area not structured electronically.

17. (Currently Amended) The process according to claim 11, wherein at least one of the wafers is electrically connected at a specific ~~switching points~~electric circuit point located in an electronically structured area of the wafer.

18. (Currently Amended) The process according to claim 11, wherein ~~the~~a glass paste connection formation ~~of the connections of the glass pastes~~ takes place at a temperature of less than 450°C.

19. (Currently Amended) The process according to claim ~~11 and any of the subsequent claims,~~11, wherein the electric connection of a substrate ~~(11)~~ of an SOI wafer ~~(8)~~ is implemented through at least one previously produced opening in a buried oxide layer ~~(10)~~of said SOI wafer and in an active silicon layer ~~(9), in particular the wall areas,~~ of said SOI wafer whereby at least one wall area of the at least one opening in the active silicon layer being provided with an insulating layer ~~(7a)~~ prior to the electric connection ~~(5)~~ with the conducting glass ~~solder~~paste.

20. (Currently Amended) A process for ~~the~~ firm connection of processed semiconductor wafers, thereby connecting ~~system wafers (1) supporting microelectromechanical or~~a system wafer carrying micro-electromechanical or first electronic structures ~~(3)~~ with a cover ~~wafers (2)~~wafer, carrying second electronic structures, wherein in an operation of ~~a~~said mechanically

firm connecting ~~both~~ electrically insulating connections and electrically conducting connections are produced between the semiconductor wafers, ~~having~~ the ~~steps~~method comprising:

applying structured layers of electrically non-conducting and electrically conducting glass pastes on ~~respectively one of the~~ two wafer sides of said wafers to be connected with each other;

conditioning and premelting of the ~~glasses~~glass pastes;

geometrical alignment of the wafers ~~to be~~for being connected;

joining of the aligned wafers at a processing temperature of the glass pastes using a mechanical pressure.